

# A Beginner's Guide to DesignLab— Schematics, PSpice, and Probe

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## Abstract

This short note introduces DesignLab which includes circuit simulation package PSpice. This note is brief and a detailed discussion can be found in various books on SPICE3[6] and PSpice [1, 5, 3].

# 1 Introduction

PSpice is a circuit simulation package. It is a commercial version of the legendary SPICE3 package (SIMULATION PROGRAM WITH INTEGRATED CIRCUIT EMPHASIS) developed in the 70s. What normally goes by the name PSpice is actually an integration of three packages. The first one is a Schematics capture program. This program enables the user to graphically build circuits from a parts bin. The circuits developed using Schematics are saved as .sch files. This circuit information is then converted to a .cir (netlist) file which forms input to the package PSpice. The netlist file .cir is then processed by PSpice and the requested simulation is performed. The results of the simulation are output to a .out file and a .dat file. Finally Probe is used to plot the data from .dat file. MicroSim, the vendors and developers of these packages, have named the suite of these packages as DesignLab.

To use DesignLab effectively, the user must first and foremost know *what they want* to do and then they must know how to use the DesignLab to do *what they want* to do. This document is an attempt to give a start in the use of DesignLab.

## 1.1 Installation

To install the package is simple. The ftp distribution comes with a self-extracting and self-installing binary. The cd-rom distribution has many more features in it; particularly the pdf format manuals. To install from it, dbl-clk on setup.exe and choose the PSpiceAD option. The programs Schematics, PSpice, and Probe are normally installed in the DesginLab folder.

## 1.2 Suffixes

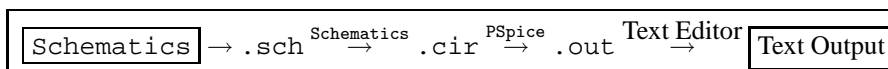
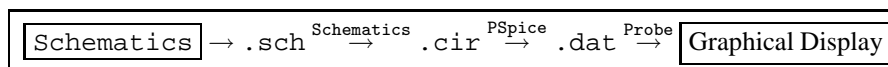
For a quick reference power-of-ten suffixes used by PSpice are given in Table 1.

SPICE3	Metric Prefix	Value
F	<i>femto-</i>	$10^{-15}$
P	<i>pico-</i>	$10^{-12}$
N	<i>nano-</i>	$10^{-9}$
U	<i>micro-</i>	$10^{-6}$
M	<i>milli-</i>	$10^{-3}$
K	<i>kilo-</i>	$10^3$
MEG	<i>mega-</i>	$10^6$
G	<i>giga-</i>	$10^9$
T	<i>tera-</i>	$10^{12}$
MIL	<i>milli-inch</i>	$25.4 \times 10^{-6}m$

Table 1: SPICE3 Prefix Notation

SPICE3 suffixes are case *insensitive*; k and K mean the same. Also note that *F* stands for *femto-* and not Farads; a  $1F$  capacitor to SPICE3 is  $10^{-15}$  Farad capacitor. Also note that both M and m mean *milli*; mega- is MEG or meg. Alphabets other than the ones used as suffixes (Table 1) are ignored whenever they follow a number, also alphabets following a suffix are ignored; e.g.,  $1mH$  is  $10^{-3}$  Henry,  $1uF$  is  $10^{-6}$  Farads, but  $10F$  for SPICE3 is  $10 \times 10^{-15}$  Farads,  $10\Omega$  resistor is  $1\Omega$ .

The normal sequence of programs to simulate a circuit is shown below. It is not necessary to use Schematics to create the .cir file; the netlist file can be created just as easily using a text editor.



## 2 Parts in Schematics

Schematics has almost all the parts that you are likely to use. To draw a schematic for analysis start the Schematics program, open the Parts Browser: Draw → Get New Part or CTRL-G. A dialog box as shown in Figure 1 will appear. Click on any part name in the left hand side box and its picture appears in the right hand side box and its description appears in the box above it. If you can't see the picture click on **Advanced>>** and the picture should appear.

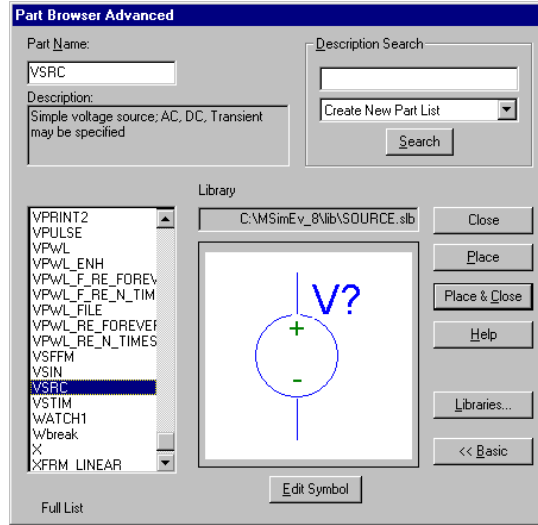


Figure 1: Parts Selection Dialog Box

You will see that the parts are listed in an alphanumeric order. To go to a particular part, click on the part list box and type the first letter of the part name and the selection dialog will take you to the first part in the list starting with that number or alphabet. To learn how to locate the part you are looking for try **Help** in the Part Browser. A list of a few often needed parts is given in Table 2.

Part Name	Description	Part Name	Description
R	Resistance	C	Capacitance
L	Inductance	K	Mutual Coupling
VSRC	Voltage Source (DC, AC, & Transient)	ISRC	Current Source (DC, AC, & Transient)
E	Voltage-Controlled Voltage Source	F	Current-Controlled Current Source
G	Voltage-Controlled Current Source	H	Current-Controlled Voltage Source
Dxxx	Diode	Qxxx	Bipolar Transistor
S	Voltage-Controlled Switch	W	Current-Controlled Switch
BUBBLE	Node Label (dbl-clk to label)	AGND or EGND	Ground (node 0)

Table 2: Parts Table with Some Frequently Used Parts

Select the part you want and click on **Place**. The part now attaches itself to the cursor; take the cursor to the schematic sheet and click on it to place the part; click the right mouse button to release the part. In this way pick up all the parts. Once the parts are picked they can be copied, cut, and pasted like in normal editors. **Description Search** box in Figure 1 is very useful. Suppose you want to see all the parts with 'voltage' in their description; type 'voltage' in the box and search. All the parts which match the description will appear. To get back to the master list of the parts, type '\*' in the **Part Name** box.

### 2.1 Voltage & Current Source

Components VSRC and ISRC can be used for DC, AC, or transient analysis. For these two sources, three values can be specified — DC, AC, and TRAN, where DC value can be used for DC analysis, AC value can be used for AC analysis, and TRAN can be either EXP, SFFM, SIN, PULSE, or PWL.

## 2.2 Controlled Sources

As an illustration two controlled-source circuits are presented. Figure 2 shows a circuit with voltage-controlled current source. This circuit in Schematics is shown in Figure 3. The parts you need to pick are: VDC, IDC, BUBBLE, GND\_ANALOG, R, G. To connect them, get Wire from Draw → Wire or CTRL-W.

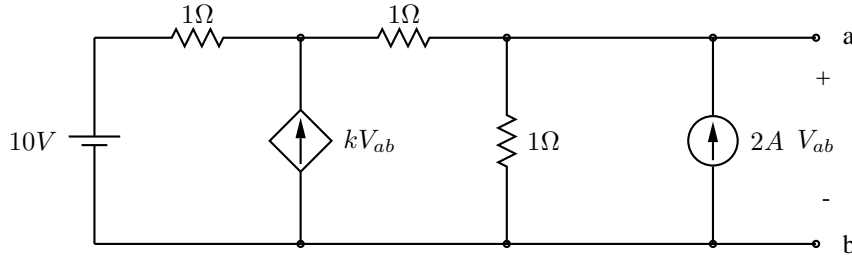


Figure 2: Circuit with Voltage Controlled Current Source

To set value of resistors, current, and voltage source, dbl-clk on the value, a box will open up, fill the value you want and close the box. To set the gain (say  $k = 2$ ) of the controlled source in Figure 3, select the source G and then Edit → Attributes or dbl-clk on the part G. A dialog box opens up; set the value of Gain = 2 and Save Attributes. Note how bubbles are used to label the terminals. Two terminals are labelled 'a' and 'b' each. All the terminals with the same label have the same potential. This means that in Figure 3 both the terminals labelled 'a' have the same potential. This feature keeps the schematic clean.

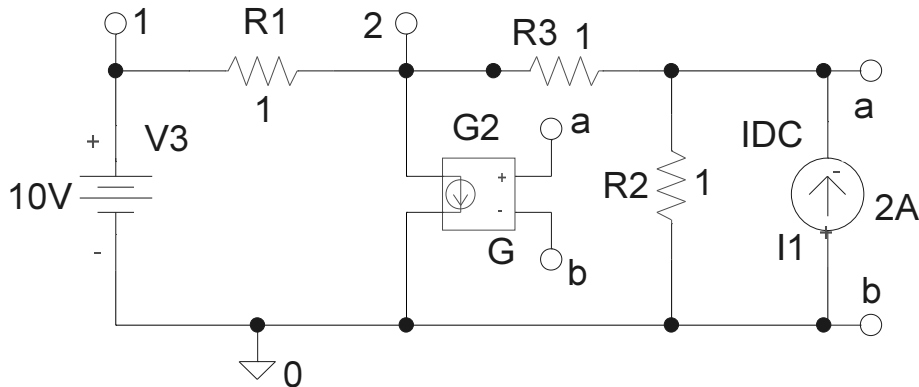


Figure 3: A VCCS Circuit in Schematics

To analyse the circuit draw it as shown in Figure 3 and then setup the analysis. In this case it will be the Bias Point Detail: Analysis → Setup → click on the box next to Bias Point Detail, OK, etc. Then run the simulation Analysis → Simulate or F11. If you have drawn the schematic correctly a PSpice window will appear on the screen. Once the simulation is complete go to File → Examine Output in PSpice or Analysis → Examine Output Schematics and have a look at the analysis.

Figure 4 shows a circuit with current-controlled current source. This circuit in Schematics is shown in Figure 5. As an exercise perform an analysis similar to the one above for the circuit Figure 5. What is  $V_a$ ?

Next we discuss four most important type of analyses. Each type of analysis is demonstrated using an example.

## 3 AC Sweep and Frequency Response

Figure 6 shows a simple RC circuit. Here  $V_1$  is a sinusoidal voltage  $1 \times \sin(2\pi ft)$ . We would like to know the relationship between the input voltage  $V_1$  and the output voltage across the capacitor  $V_2$  as a function of the input sinusoidal voltage frequency at steady-state.

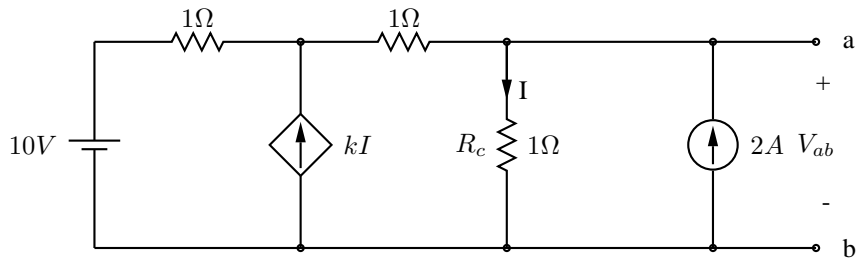


Figure 4: Circuit with Current Controlled Current Source

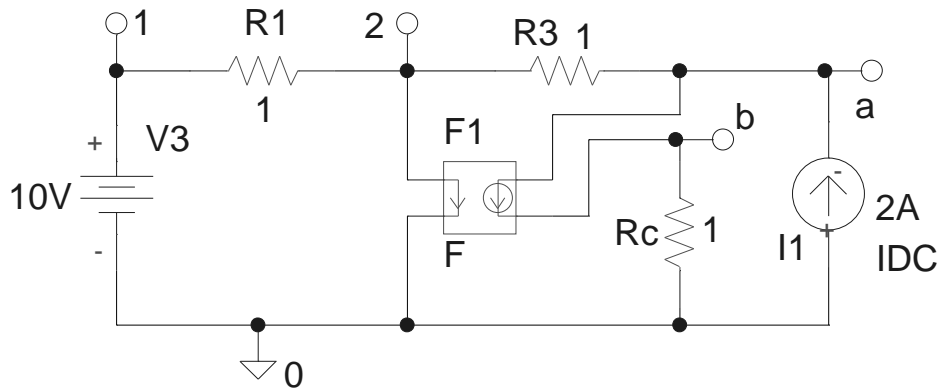


Figure 5: A CCCS Circuit in Schematics

### 3.1 Schematics

To draw the circuit shown in Figure 6 start the *Schematics* program from within the *DesignLab* program group. Once the schematic window comes up go to the *Draw* menu and select *Get New Parts* (short cut CTRL-G). The parts you need to pick are: *VAC*, *BUBBLE*, *GND\_ANALOG*, *R*, *C*. Place the parts as you see in Figure 6 and then to connect them, get the wire from the *Draw* menu (also CTRL-W). Connect the components. To label the *BUBBLE* *dbl-clk* on it and then type the label you want that node to have. If you don't label *BUBBLE* the *Schematics* → *netlist* program will complain. Labels can be any alphanumeric string. You will notice that the resistor and the capacitor don't have the values you want for them. To set the desired values *dbl-clk* on the 'value' of the part and then key in the desired value in the dialog box. You will see that there is no place to set frequency of the AC voltage source *V1*; you can only set its magnitude. The reason being that this source is used only for AC Sweep and the range of frequencies this source takes on have to be specified in analysis setup step discussed in the next section.

To get the part with "V" inside a circle and an arrow connected to node 2, go to the *Markers* in the menu and choose *Mark Voltage/Level* (CTRL-M) and place it appropriately. These markers do the job of voltmeters and ammeters.

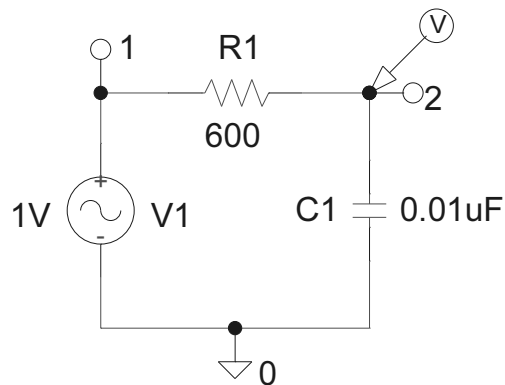


Figure 6: An RC circuit and AC sweep

Once the simulation is complete you can change the position of the markers and the levels at the corresponding position will be displayed in the Probe window. Now you can save the circuit. Remember that every schematic needs a ground with a node label 0, without this PSpice will complain of floating terminals and will not perform the simulation.

### 3.1.1 Analysis Setup

With the circuit captured using the Schematics we now need to decide how to tell PSpice to get the frequency response. PSpice can perform several types of analyses. By choosing Analysis → Setup you are presented with the choices shown in Figure 7. We need to decide which analysis will suit our needs.

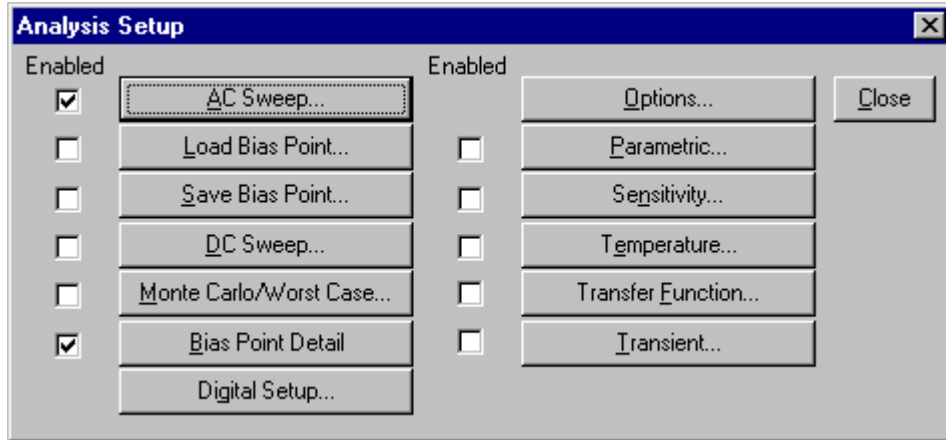


Figure 7: Analysis Setup Menu

Before we do that let us have a quick look at the phasor analysis. From theory we know that the output voltage will be of the same frequency as the input voltage frequency but of different magnitude and phase. In other words to know the steady-state output voltage completely it's sufficient to know its magnitude and phase shift. Phasor analysis is a simple way to get this information. For the circuit in Figure 6, in the language of phasors (Let  $\angle \vec{V}_1 = 0$ ):

$$\vec{V}_2 = \frac{\frac{1}{j\omega C_1}}{R_1 + \frac{1}{j\omega C_1}} \vec{V}_1 = \frac{\vec{V}_1}{1 + j\omega R_1 C_1}$$

In general the complex number  $V_2$  will be a function of  $\omega$ .

$$|\vec{V}_2| = \frac{|\vec{V}_1|}{\sqrt{(1 + (\omega R_1 C_1)^2)}} \text{ and } \angle \vec{V}_2 = \tan^{-1} \left( \frac{-\omega R_1 C_1}{1} \right) \quad (1)$$

From equation (1) it can be seen that magnitude and phase of  $\vec{V}_2$  are dependent on the frequency. An evaluation of  $\vec{V}_2$  for various frequencies is called AC Sweep. On clicking the AC Sweep box of the menu in Figure 7, a box as in Figure 8 will open. To setup our analysis here are the steps: Analysis → Setup → AC Sweep → (Decade; Pts/Decade: 20; Start Freq: 1k; End Freq: 100k) → OK etc.

Whenever we ask PSpice to perform AC analysis it sets all the DC sources and other time-varying sources to zero. It considers only the sources for which an AC value has been specified and sweeps the frequency of all the AC sources together.

Having setup the analysis, to run the simulation: Analysis → Simulate (F11-key).

### 3.1.2 THE OUTPUT FILE

PSpice writes all its output in .out file. There is much important information there and you should have a look in it after the simulation is complete. To open the .out file: in the PSpice window File → Examine Output or use an editor to open it; it's a text file. If there is an error in the netlist file or the simulation doesn't complete the first place to look for the exact description of errors is in the .out file.

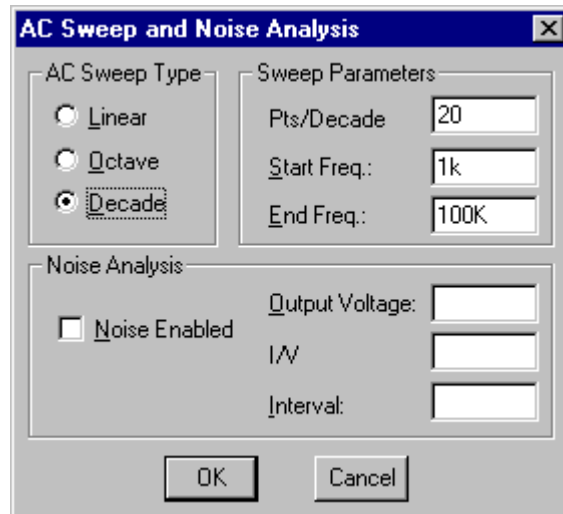


Figure 8: AC sweep Analysis Setup Menu

### 3.2 Probe

After PSpice successfully completes the simulation it should start Probe automatically. In case it doesn't then start Probe from the 'program control window' and then (File) → Open the corresponding .dat file. In Probe the following sequence of commands will generate the plot shown in Figure 9. From the Probe menu:

Trace → Delete All

Trace → Add → P() (right panel) → V(2) (left panel)

Plot → Add Plot

Trace → Add → M() (right panel) → V(2) (left panel)

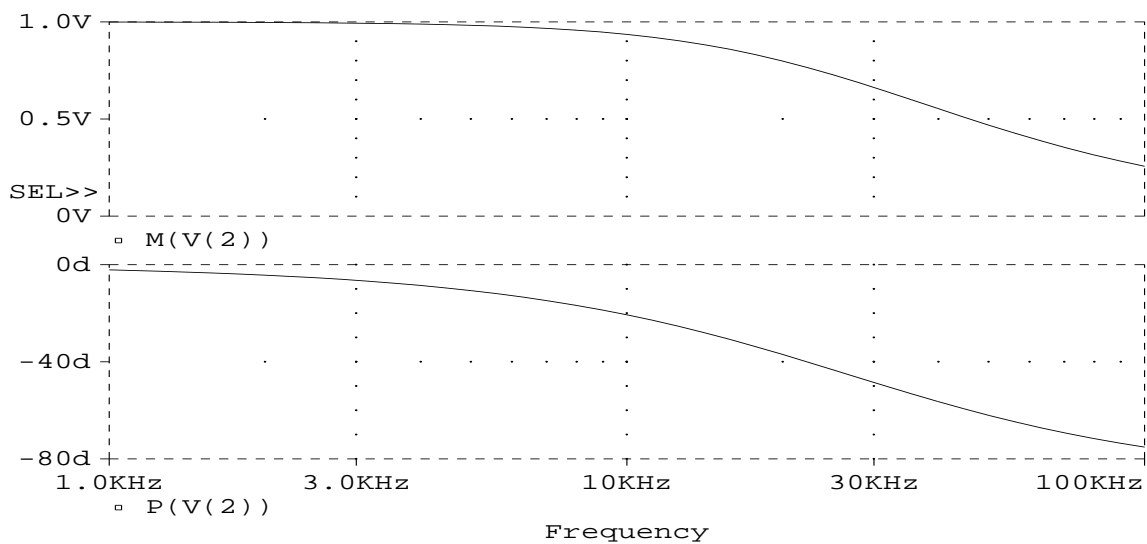


Figure 9: RC circuit and AC sweep output using probe

## 4 Transient Analysis

Transient analysis is performed to simulate the time response of circuits. A familiar example is when a square wave is applied to a circuit with energy storage elements. In the following we will simulate the response of an RC circuit shown in Figure 10 due to a square wave.

## 4.1 Schematics

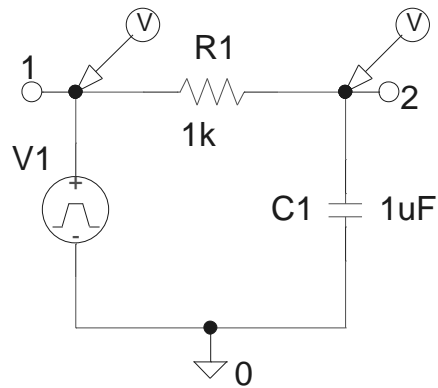


Figure 10: An RC circuit and Transient Analysis

Draw the schematic shown in Figure 10:

Draw → Get New Part → VPULSE

Select the voltage source V1 then either Edit → Attributes or dbl-clk and set the attribute values as follows:

DC=0; AC=0; V1=0; V2=5V; TD=0s; TR=1ns; TF=1ns; PW=5ms; PER=10ms

The pulse voltage waveform is shown in Figure 11. Drawing other components in the schematic Figure 10 is by now familiar to you.

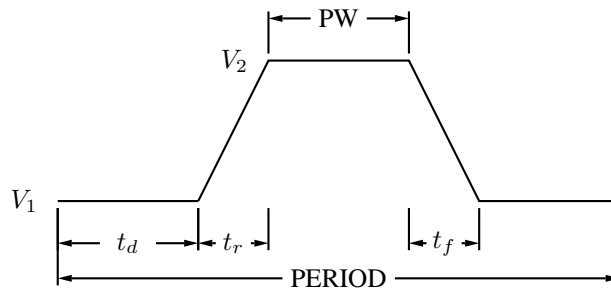


Figure 11: Pulse Voltage Source Specifications

## 4.2 Analysis Setup

Analysis → Setup → Disable all the previously selected analyses (except may be Bias Point Detail). Then setup the Transient analysis as follows:

Transient → (Print Step: 0.1ms; Final Time: 20ms) → OK etc.

While performing the transient analysis PSpice sets all the AC voltage sources to zero. For a transient analysis there must be at least one DC source or a time varying source. To set an initial voltage on a capacitor dbl-clk on the capacitor plates; a dialog box will open; change the value of the IC attribute to the value you want to set. Similarly the IC attribute of an inductor can be set to any initial current.

Now start the simulation by either pressing F11-key or Analysis → Simulate.

## 4.3 Probe

The plot in Figure 12 should now show in a Probe window once the simulation is complete. If it doesn't show on its own then:

Trace → Add → V(1) → OK → Trace → Add → V(2)

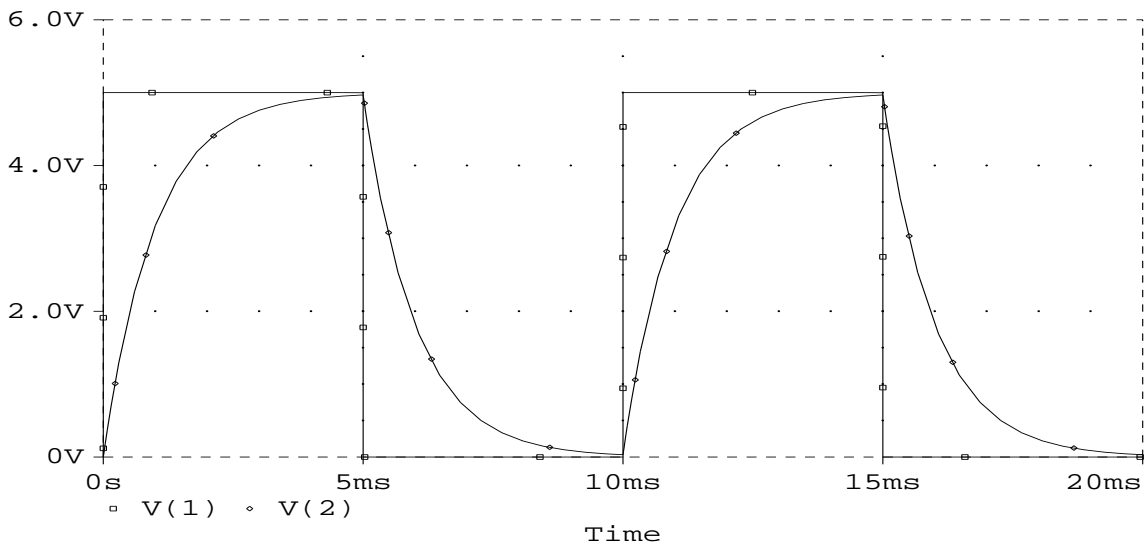


Figure 12: RC circuit and Transient analysis output using probe

## 5 DC Sweep

To simulate a circuit for several values of DC voltage or current, DC sweep can be used. DC sweep is used in the following example to trace the transfer characteristics of an inverting amplifier shown in Figure 13.

### 5.1 Schematics

Draw the schematic shown in Figure 13.

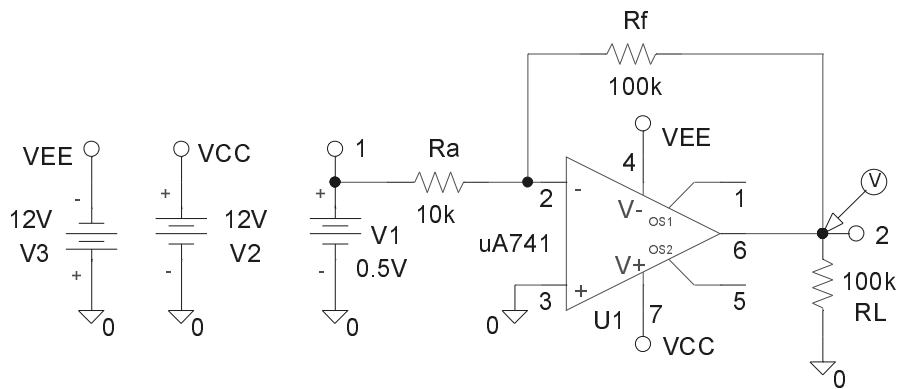


Figure 13: Direct coupled amplifier and DC sweep

### 5.2 Analysis Setup

Setup the DC analysis as follows:

Analysis → Setup → DC Sweep → (Swept Var. Type: Voltage Source; Name: V1; Sweep Type: Line Start Value: -1.5; End Value: 1.5; Increment: 0.1) → OK etc.

### 5.3 Probe

In Probe the following sequence of commands will generate the plot you see in Figure 14. After PSpice successfully completes the simulation it should start Probe automatically. In case it doesn't, start Probe and (File) → Open the corresponding .dat file. Then from the Probe menu:

Trace → Delete All → OK → Trace → Add → V(2)

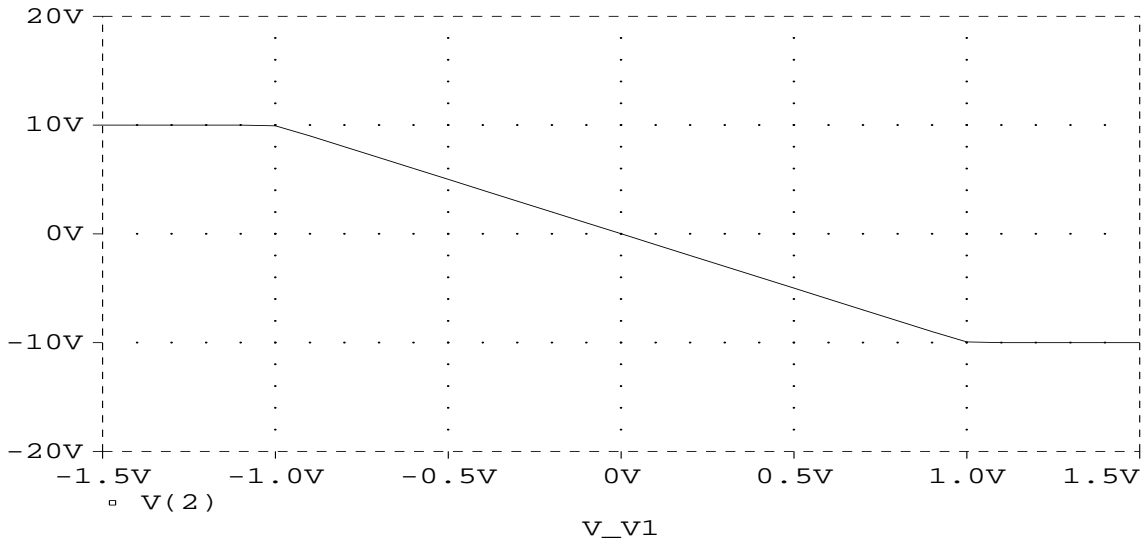


Figure 14: Direct coupled amplifier and DC sweep output using probe

## 6 PARAM Part – Parametric Analysis

At times it is desirable to simulate the circuit behaviour for changing component values. Parametric Analysis can be used in conjunction with AC Sweep, DC Sweep, and Transient Analysis. To do so we must first declare it to PSpice that a particular component's value is to be varied during the analysis and then setup an appropriate analysis. This is illustrated in the next example. In this example we want to find the value of the resistor  $R_2$  for maximum power transfer across it from the circuit.

### 6.1 Schematics

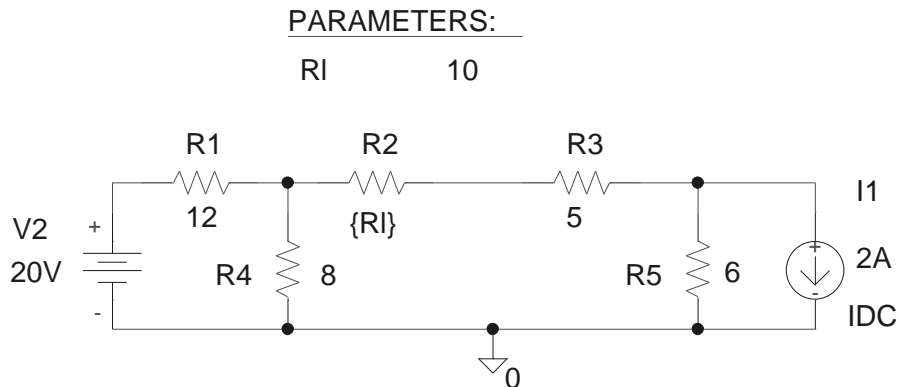


Figure 15: Maximum Power Transfer Parametric analysis

Pick the parts from the Part Browser to set most of the circuit as you see in Figure 15. The PARAMETERS: block on the top is the part PARAM. Get this part and put it somewhere on the schematic. Now dbl-click on the value of the R2 resistor. This default value is normally 1k. In the dialog box type {R1}. You can type any name there but it has to be within curly braces. The curly braces tell Schematics that this is a parameter whose value will be set by the PARAMETERS: block. Now dbl-click on the PARAMETERS: block and a dialog box PM1 PARTNAME: PARAM opens up. In that box set the value of NAME1=R1 and VALUE1=10 (no curly braces around R1 here). This value of '10' is known as the nominal

value. If any analysis is performed where the R1 parameter is not varied then the nominal value is used for that analysis. From the PM1 PARTNAME: PARAM dialog box it can be seen that we can declare upto three parametric parts using one PARAM block.

## 6.2 Analysis Setup

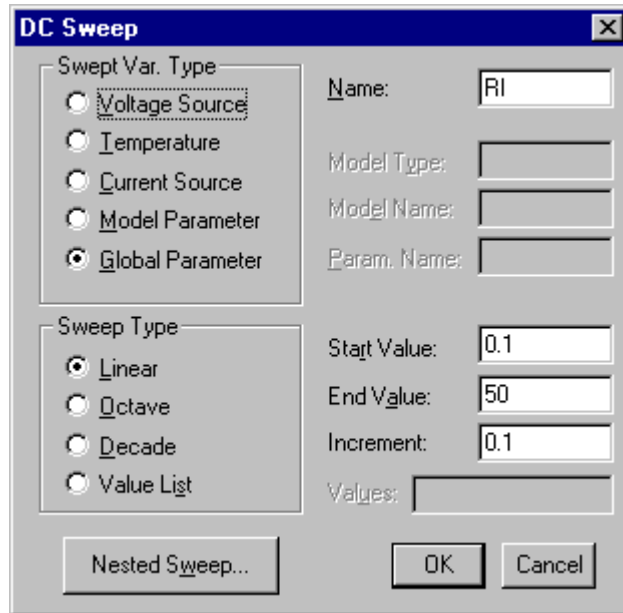


Figure 16: Parametric Analysis Setup Menu

Analysis → Setup → DC Sweep → (Swept Var. Type: Global Parameter; Name: R1; Sweep Type: Linear; Start Value: 0.1; End Value: 50; Increment: 0.1) → OK etc. as shown in Figure 16.

## 6.3 Probe

In Probe the following sequence of commands will generate the plot you see in Figure 17. After PSpice successfully completes the simulation it should start Probe automatically. In case it doesn't start Probe and (File) → Open the corresponding .dat file. Then from the Probe menu:

Trace → Delete All → OK → Trace → Add → I(R2)\*I(R2)\*R1 (in the Trace Expression box)

Tools → Cursor → Display

Tools → Cursor → Max

## 7 Probe

Probe is a plotting package which comes bundled with DesignLab. In a PSpice script (.cir file) you can either give a command to save the entire simulation data or a few specified voltages and currents. For example

```
.probe
```

will save the entire simulation data and

```
.probe v(2) v(5) I(R1)
```

will save the data for voltages at nodes 2 and 5 and the current through resistor R1. If you are using Schematics to build the .cir file then it will automatically include statements to write the entire simulation data to a .dat file.

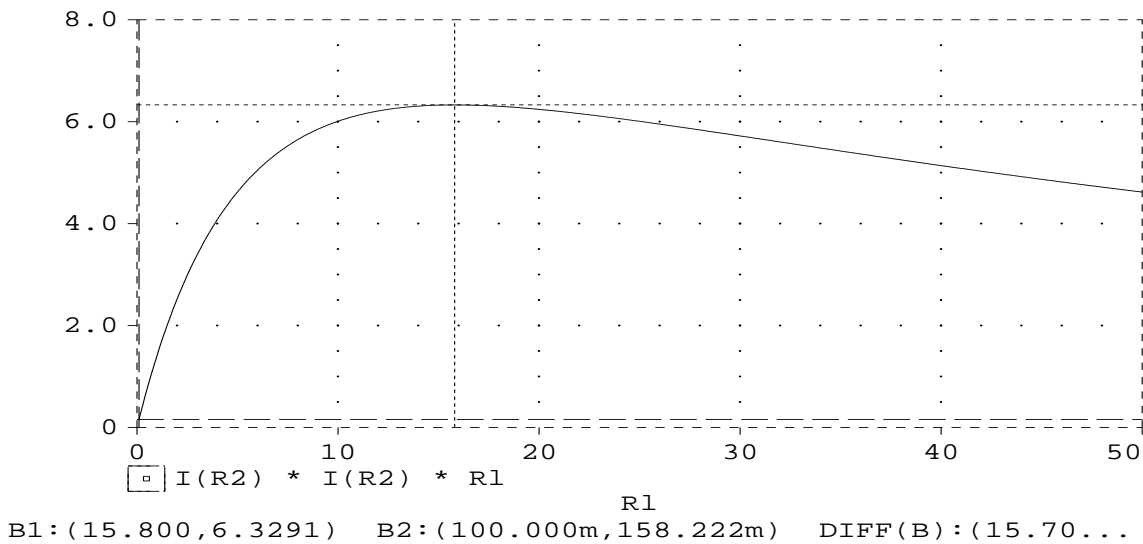


Figure 17: Maximum Power Transfer Parametric analysis output using probe

## 7.1 Trace → Add

Probe automatically plots the data on which you have either attached a voltage or a current marker in the schematic. Often you would want to plot data and functions of data at other locations. Probe Trace → Add brings up the dialog box shown in Figure 18. On the right panel it displays the functions available to the user. Let us assume that we have just performed an AC sweep and now the data from that sweep has to be plotted. The currents and voltages at each node are stored in separate arrays. In the language of Probe,  $V(2)$  is an array of voltages at node 2 for different frequencies of the AC sweep. `clk` on `DB()` in the right hand panel of Figure 18 and `DB()` appears in the Trace Expression dialog box and the cursor is in between the round brackets. Now if you `clk` on  $V(2)$  the Trace Expression dialog box shows `DBV(V(2))`. This means that Probe will take each individual element of  $V(2)$  take its  $20 \log_{10}()$  and then plot it as a function of frequency.

Here is a brief description of a few modifiers and the functions that you can use with Probe. To find out more about the functions click on the `Help` box in the dialog box shown in Figure 18 then Defining Analog Trace → Expressions → functions.

Modifier	Effect	Example
M	Magnitude (The default)	VM(2) or M(V(2))— Magnitude of V(2)
P	Phase	VP(2) or P(V(2)) — Phase of V(2)
R	Real Part	VR(2) or R(V(2)) — Real part of V(2)
I	Imaginary Part	VI(2) or I(V(2))— Imaginary part of V(2)
DB	20 times log of value	VDB(2) or DB(V(2))— $20 \log_{10}(V(2))$

Function	Expression	Comment
$sgn(x)$	1 for $x > 0$ , -1 for $x < 0$ , 0, $x = 0$	
$m(x)$	Magnitude of $x$	$x$ may be complex
$p(x)$	Phase of $x$	In degrees
$r(x)$	Real part of $x$	
$img(x)$	Imaginary part of $x$	
$g(x)$	Group delay of $x$	
$d(x)$	Derivative of $x$	With respect to X-axis
$s(x)$	Integral of $x$	With respect to X-axis
$avg(x)$	Running average of $x$	With respect to X-axis
$avg(x, d)$	Running average of $x$ from $x - d$ to $x$	Over range of X-axis
$rms(x)$	Running RMS average of $x$	Over range of X-axis
$db(x)$	Magnitude of $x$ in decibels	
$min(x)$	Minimum of real part of $x$	
$max(x)$	Maximum of real part of $x$	

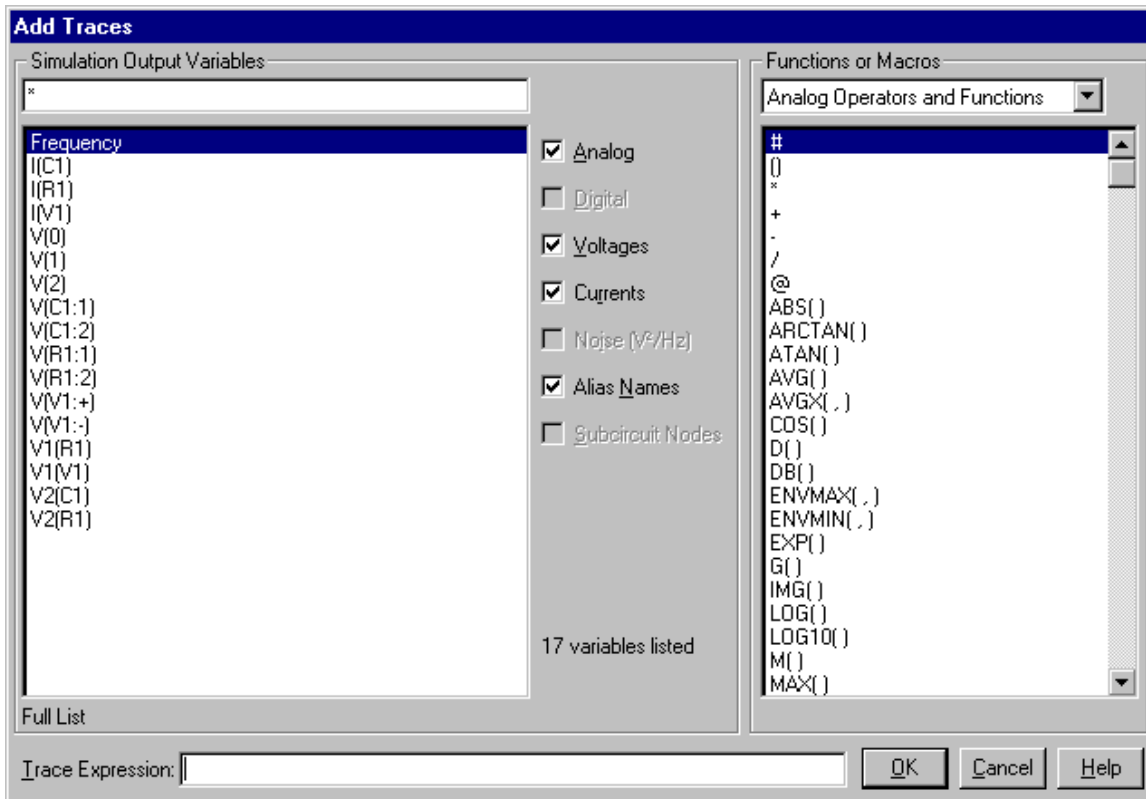


Figure 18: Probe 'Add Trace' Dialog Box

## 7.2 Other Features

Many times it so happens that not all variables of interest can be plotted on the same plot. In that case you can request Probe to open a new plot in the window. This is done by `Plot` → `Add Plot`. Clicking a plot window selects it and the following Probe commands apply to that plot.

Probe has many more useful commands; you should explore the `Probe` menu to find out how to label axes, annotate the graphs etc. You will often repeat the `simulate` → `plot` cycle. To plot the same combination of variables you can log the Probe commands using the `Log Commands` menu item under the `File` Menu and then replay them.

## 8 SPICE Model Parameters

The following description applies when creating netlist directly without using `Schematics`. But it will also be a great help when using the `break parts` to simulate semiconductor devices which don't come with `DesignLab`.

### 8.1 The Model Statement

To include semiconductor devices in `PSPICE` or `SPICE3` we have to tell the simulator what are the characteristics of the device. Different semiconductor devices have different properties unlike say a resistor. To specify a resistor all you have to do is to tell what's its resistance and the job is done. `SPICE3` has default values for all the semiconductor devices so if you want to do some simple analysis you can tell the program that you are happy with the default values and in that case your `.model` statement can be very simple. Here are a few sample pairs; the first statement gives the node connection of the semiconductor device and the second is the `.model` statement.

```
D1 1 2 defd ; Diode (node sequence p-side n-side)
.model defd D ; default diode model
Q1 1 2 3 defq ; NPN transistor (node sequence C B E)
.model defq NPN ; default NPN model
Q2 1 2 3 defq2 ; PNP transistor (node sequence C B E)
```

```
.model defq2 PNP ; default PNP model
J1 1 2 3 defj ; N-channel junction FET (node sequence D G S)
.model defj NJF ; default NJF model
J2 5 6 7 defjp ; P-channel junction FET (node sequence D G S)
.model defjp PJF ; default PJF model
M1 1 2 3 4 defm ; N-channel MOSFET (node sequence D G Source Substrate)
.model defm NMOS ; default NMOS model
M2 1 2 3 4 defmp ; P-channel MOSFET (node sequence D G Source Substrate)
.model defmp PMOS ; default PMOS model
Note that the in-line comments following ';' are allowed only in PSpice.
There are a few important points to remember about the above statements.
```

- The first letter of every device should be exactly as given, e.g., when you want to include a BJT the first letter should be Q, etc.
- The node sequence also is fixed. For example in the BJT declaration the first node after Qxxx has to be the collector, then the base, and finally the emitter.
- defq in the declaration of Q1 above tells the program that the characteristics of the device connected here should be looked up in the .model statement for defq. There is no restriction on the name you choose for the model.
- The .model statement for a particular type of device should use only a particular word. For example, an NPN BJT has to be declared by the letters NPN. The second word after .model above is the word reserved for that particular device. Looking at the above statements you can get an idea of which word is used for which device. Many more devices than shown above can be simulated with PSpice, for a complete list see [5] or browse through the Schematics parts library.
- If you want to give the device values other than the default ones then you have to specify them following the reserved word as done in the three scripts we presented before. To get an idea of what the default settings are look in the .out file after performing a simulation. To find out which parameters mean what have a look in the text-book [2, pp 185-187].

## 8.2 Break Parts

Schematics makes provision for including parts which are not available in its parts library. Parts whose parameters can be changed are called break parts. The difference between other parts and break parts is as follows. Other parts cannot be saved in a different name and when you change their characteristics the record in the master file eval.lib gets changed. But the break parts can be saved under a different name and so the change in device parameters is specific to the new part you have created.

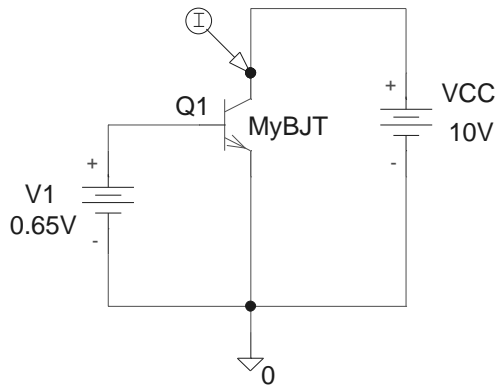


Figure 19: BJT Characteristics

To create Q1 shown in Figure 19 choose Get New Part (Ctrl-G) from the Draw menu from within the Schematics, then choose part 'QbreakN' and place it in the circuit. Now highlight the part 'QbreakN' and then Edit → Model. Click on Edit instance Model (Text)..., a window appears with the contents shown in Table 3. You can edit the '.model' command so that it is something like you see in the script in Table 4. This process will save the model for you in a .lib file with the same name as the name you give to the circuit. You can either directly change the model parameters by editing the .lib file or repeat the process given above to change the model parameters.

Remember that the PSpice has provided 'break' parts for you to copy and modify them to your requirements. The first time the Model Editor window will come up you will see the following.

```
.model Qbreakn NPN
*$
```

Table 3: The Model Editor Dialog Box

You can change Qbreakn to say MyBJT or any other name that takes your fancy. The values of the BJT parameters shown in Table 6 can also be keyed in as shown below in Table 4. Note that a comma or a newline or a space can be used to separate two values. After you edit the parameter values the Model Editor window might look something like seen in Table 4.

```
.model MyBJT NPN
IS = 1e-15, BF=300
VAF=200 RB=0.01 RE=0.0001
TF=1n
CJE=1.2f
MJE=1.4
*$
```

Table 4: The Edited Model Editor Dialog Box

Nested DC Analysis is used to vary VCC and V1 in Figure 19 to get the transistor characteristics shown in Figure 20. In Figure 20 collector current for changing VCC is plotted; V1 is held constant for each curve in the plot. As an exercise see if you can setup the analysis and get a similar plot.

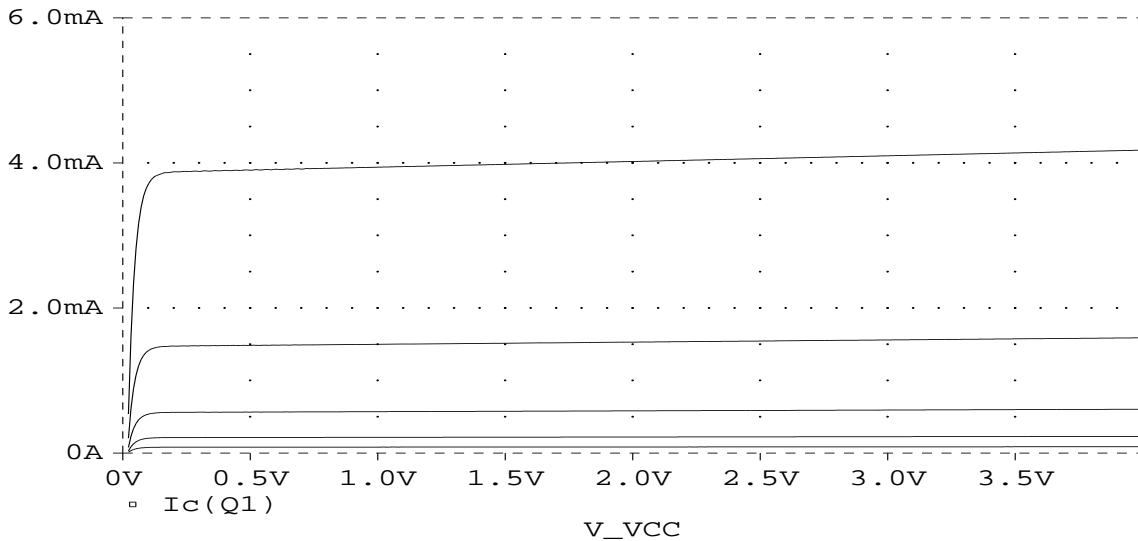


Figure 20: BJT Characteristics output using probe

### 8.3 More SPICE3

As described above you can use break-parts to simulate circuits with parts not in the Schematics library. Alternatively you can copy the models from eval.lib which comes with PSpice; give models new names and change the model parameters appropriately. If you are using PSpice scripts you can create a library of your own. Let's say you call it mylib.lib then you can include the models in the library by using the following line:

```
.LIB "path\mylib.lib"
```

You can also read in a PSpice script into the current script by including:

.INC "path\filename"

If you are using Schematics then the library files etc. can be set from the Analysis Menu. The .INC and .LIB commands are not available in SPICE3.

Most of the manufacturers supply model files for the components they manufacture to make it easy for people using SPICE3 to simulate circuits with their parts. You can search the net for manufacturer's site and then download the models. One good site to check out is the MicroSim site <http://www.microsim.com>.

## 9 Mathematical Models of Semiconductor Devices

This section gives a quick reference to the mathematical models of three often used devices. The correspondence between the symbols used in text-books [2] and the SPICE3 symbols are given in the following Tables.

### 9.1 Semiconductor Diode

$$I_{\text{forward}} = I_S e^{\frac{V_j}{N V_T}} \text{ and } I_{\text{reverse}} = I_B V e^{\frac{-(V_j + BV)}{V_T}}$$

SPICE Symbol	Text Symbol	Description	Units	Defaults
IS	$I_s$	saturation current	amp	$10^{-16}$
N		emission coefficient		1
BV		reverse breakdown "knee" voltage	amp	$\infty$
IBV		reverse breakdown "knee" current	volt	$10^{-10}$
RS		parasitic resistance	ohm	0
CJ0	$C_{j0}$	zero-bias $p$ - $n$ capacitance	farad	0
VJ	$\phi_0$	$p$ - $n$ potential	volt	1
EG	$E_G$	bandgap voltage (barrier height)	eV	1.11

Table 5: Semiconductor Diode Parameters

Zener diodes are included by setting the reverse breakdown voltage  $BV$  to the zener breakdown voltage value.

### 9.2 Bipolar Junction Transistor

$$g_m = \frac{I_C}{V_T}; r_\pi = \frac{\beta_F}{g_m}; C_b = \tau_F g_m; r_o = \frac{V_A}{I_C}; r_\mu = \beta_F r_o; C_{je} \approx 2 C_{je0};$$

$$C_\pi = C_b + C_{je}; C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{\psi_{0c}}\right)^{n_c}}; C_{cs} = \frac{C_{cs0}}{\left(1 + \frac{V_{CS}}{\psi_{0s}}\right)^{n_s}};$$

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} (1 + \lambda V_A) \quad (2)$$

### 9.3 Junction Field Effect Transistor

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 + \lambda V_{DS}) \quad (3)$$

$$r_o = \frac{1}{\lambda I_d} \quad (4)$$

$$g_m = \frac{-2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right) \quad (5)$$

$$g_{m0} = \frac{-2I_{DSS}}{V_P} \quad (6)$$

SPICE Symbol	Text Symbol	Description	Units	Defaults
IS	$I_s$	Transport saturation current	amp	$10^{-16}$
BF	$\beta_F$	Maximum forward current gain		100
BR	$\beta_R$	Maximum reverse current gain		1
VA	$V_A$	Forward Early voltage	volt	$\infty$
RB	$r_b$	Base Series resistance	$\Omega$	0
RE	$r_{ex}$	Emitter Series resistance	$\Omega$	0
RC	$r_c$	Collector Series resistance	$\Omega$	0
TF	$\tau_F$	Forward transit time	sec	0
TR	$\tau_R$	Reverse transit time	sec	0
CJE	$C_{je0}$	Zero-bias base-emitter depletion capacitance	F	0
VJE	$\psi_{0e}$	Base-emitter junction built-in potential	volt	0.75
MJE	$n_e$	Base-emitter junction-capacitance exponent		0.33
CJC	$C_{\mu 0}$	Zero-bias base-collector depletion capacitance	F	0
VJC	$\psi_{0c}$	Base-collector junction built-in potential	volt	0.75
MJC	$n_c$	Base-collector junction-capacitance exponent		0.33
CJS	$C_{cs0}$	Zero-bias collector-substrate depletion capacitance	F	0
VJS	$\psi_{0s}$	Collector-substrate junction built-in potential	volt	0.75
MJS	$n_s$	Collector-substrate junction-capacitance exponent		0

Table 6: Bipolar Transistor Parameters

SPICE Symbol	Text Symbol	Description	Units	Defaults
VTO	$V_P$	Threshold voltage (pinch-off voltage)	volt	-2
LAMBDA	$\lambda$	Channel-length modulation parameter	$\text{volt}^{-1}$	0
BETA	$\frac{I_{DSS}}{V_P^2}$	Transconductance parameter	$\text{amp/volt}^2$	$10^{-4}$
RD	$r_d$	Series drain resistance	$\Omega$	0
CGS	$C_{gs0}$	Zero-bias gate-source junction capacitance	F	0
PB	$\psi_0$	Gate-channel junction built-in potential	volt	1
CGD	$C_{gd0}$	Zero-bias gate-drain junction capacitance	F	0

Table 7: JFET Parameters

## 9.4 Metal Oxide Semiconductor Field Effect Transistor

$$I_D = \frac{k'}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \quad (7)$$

$$r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \quad (8)$$

$$g_m = k' \frac{W}{L} (V_{GS} - V_t) \quad (9)$$

$$k' = \mu_n C_{ox} = \mu_n \frac{\epsilon_{ox}}{t_{ox}} \quad (10)$$

## References

- [1] James G. Gottling. *Hands-On PSpice*. Houghton Mifflin Co., 1995. ISBN 0-395-69916-9.
- [2] Paul R. Gray and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley and Sons, Brisbane, 3rd edition, 1993.
- [3] Marc E. Herniter. *Schematic Capture with MicroSim PSpice*. Prentice Hall, NJ, 2nd edition, 1996. ISBN: 0-13-233982-X.

SPICE Symbol	Text Symbol	Description	Units	Defaults
L	$L$	Channel length	m	$100\mu m$
W	$W$	Channel width	m	$100\mu m$
VTO	$V_t$	Threshold voltage with zero source-substrate voltage	volt	-2
KP	$\mu C_{ox} = \frac{\mu \epsilon_{ox}}{t_{ox}}$	Transconductance parameter	amp/volt <sup>2</sup>	$2 \times 10^{-5}$
GAMMA	$\gamma = \frac{1}{C_{ox}} \sqrt{2q\epsilon N_A}$	Threshold voltage parameter	volt <sup>1/2</sup>	calculated
PHI	$2\phi_F$	surface potential	volt	0.6
LAMBDA	$\lambda = \frac{1}{L_{eff}} \frac{dX_d}{dV_{DS}}$	Channel-length modulation parameter	volt <sup>-1</sup>	0
CGSO	$C_{ol}$	Gate-source overlap capacitance per unit channel width	F/m	0
CGDO	$C_{ol}$	Gate-drain overlap capacitance per unit channel width	F/m	0
CJ	$C_{j0}$	Zero-bias junction capacitance per unit area from source and drain bottom to bulk (substrate)	F/m <sup>2</sup>	0
MJ	$n$	Source-bulk and drain-bulk junction capacitance exponent (grading coefficient)	F/m <sup>2</sup>	0.5
CJSW	$C_{jsw0}$	Zero-bias junction capacitance per unit junction perimeter from source and drain sidewall (periphery) to bulk	F/m <sup>2</sup>	0
MJSW	$n$	Source-bulk and drain-bulk sidewall junction capacitance exponent	F/m <sup>2</sup>	0.33
PB	$\psi_0$	Source-bulk and drain-bulk junction built-in potential	volt	0.8
TOX	$t_{ox}$	Oxide thickness	m	calculated
NSUB	$N_A, N_B$	Substrate doping	1/cm <sup>3</sup>	none
NSS	$Q_{ss}/q$	Surface-state density	1/cm <sup>2</sup>	none
XJ	$X_j$	Source, drain junction depth	m	0
LD	$L_d$	Source, drain lateral diffusion	m	0
WD	$W_d$	Source, drain lateral diffusion	m	0

Table 8: MOSFET Parameters

- [4] B. Johnson, T. Quarles, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli. *SPICE3 User's Manual*. Department EECS, University of Berkeley, CA 94720 USA, April 1991.
- [5] Paul W. Tuinenga. *SPICE: A Guide to Circuit Simulation & Analysis Using PSpice*. Prentice Hall, NJ, 3rd edition, 1995. ISBN 0-13-433780-8.
- [6] Andrei Vladimirescu. *The SPICE Book*. John Wiley & Sons, Inc., Brisbane, 1994.